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SPECIFICATION

ADDRESS PATTERN GENERATOR

BACKGROUND OF THE INVENTION

1. Field of the Invention:

The present invention relates to an address pattern generator for testing a memory, etc. which are accessed by two addresses (two-dimensions).

2. Prior Art:

An arrangement of a conventional address pattern generator will be described with reference to Fig. 4.

The conventional address pattern generator comprises a control circuit 1, first and second maximum value registers 2 and 3, a column address generator 8, a row address generator 9 and a memory 10 which is to be tested. A column address signal 20 issued by the column address generator 8 is supplied to the memory 10 as a column address. A row address signal 21 issued by the row address generator 9 is supplied to the memory 10 as a row address. A memory cell in the memory 10 is accessed by supplying a column address and a row address to the memory 10.

The arrangement of the memory cells in the memory 10 will be described with reference to Fig. 5. In Fig. 5. the memory cells A0 to A15 are arranged as a matrix. In case of accessing a memory cell A10 of the memory 10, a column address signal 20 representing a column address "010" is supplied from the column address generator 8 to the memory 10 while a row address signal 21 representing a row address "010" is supplied from the row address generator 9 to the memory 10.

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The arrangement of the conventional column address generator 8 will be described with reference to Fig. 6. The arrangement of the column address generator 8 is the same as that of the row address generator 9. The column address generator 8 comprises an operation register 8A, an adder 8B and an address register 8G. When a control circuit 1 supplies an add signal 19 to the adder 8B, the adder 8B adds the content of the address register 8G and the content of the operation register 8A. The result of addition is stored in the address register 8G and it is output from the address register 8G as the address signal 20. An address value 17 is the signal output from the first maximum value register 2 which stores therein the maximum value of the address register 8G.

The number of address bits of the memory cell to be tested is generally used as the maximum value. For example, in case of the memory having 64 bit capacity, 6 bits are used as the address bit wherein 3 bits are used for the row address and 3 bits are used for the column address. Since the address generator has a surplus number of ~~bit~~ bits compared with the capacity bit of the memory (address bit) to be tested, the number of ~~bit~~ bits to be used should be limited.

When the memory cells A0 to A15 in Fig. 5 are accessed sequentially, the column address "011" and the row address "011" are respectively stored in the first and second maximum value registers 2 and 3. The column address "000" is stored in the address register 8G of the column address generator 8 as the initial value thereof while the column address "001" is stored in the operation register 8A and thereafter the add signal 19 is supplied to the adder 8B so that the column addresses "000", "001", "010" and "011" are sequentially supplied from the address register 8G to the memory 10 as the column

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address signal 20. The row address "000" is stored in the address register 9G of the row address generator 9 as the initial value thereof while the column address "000" is stored in the operation register 9A so that the row address "000" is supplied fixedly from the row address register 9G to the memory 10 as the row address signal 21.

The memory cells A0, A1, A2 and A3 are sequentially accessed when the column and row address signals 20 and 21 are supplied to the memory 10. When the memory cells A4 to A15 are sequentially accessed after the accesses of the memory cells A0 to A3, it is necessary that the column address signal 20 should automatically represent the column address "000" and the row address signal 21 should automatically represent the row address "001". If the content of the first maximum value register 2 is supplied to the column address generator 8 and the content of the second maximum value register 3 is supplied to the row address generator 9, an add value 27, which is obtained by carrying out the logical OR between a value representing the content of the operation register 8A and the value to be obtained by inverting the content of the first maximum value register 2, is supplied to the adder 8B wherein the add value 27, the add signal 19 and the output of the address register 8G are added while the upper bits are masked.

If the result of addition in the adder 8B exceeds the content of the first maximum value register 2, a carry is generated to thereby issue a carry signal 22. The carry signal 22 is supplied to the adder 9B of the row address generator 9 whereby the output of the row address generator 9 is rendered to be +1. The masked upper bits can be removed by carrying out the logical AND between an address signal 26, which is the result of operation in the adder 8B, and a value representing the content of the first maximum value register 2. In this case, since the

add value 27 of the address becomes "101", if the next add signal 19 is supplied to the adder 8B in case the content of the address register 8G is "011", there is produced "000" as the result of the operation as an address signal 26 and at the same time a carry is generated. As a result, the row address generator 9 carries out an addition in the adder 8B including the carry signal 22 whereby the row address signal 21 is rendered to be +1.

Accordingly, the column address signal 20 is output from the column address register 8 in the order of "000", "001", "010" and "011" and is returned again to "000". The row address signal 21 is increased by + 1 starting at the initial-value "000" every time the column address signal 20 returns to "000" again so that the row address signal 21 is output in the order of "001", "010" and "011". With the operations set forth above, the memory cells A0 to A15 can be sequentially accessed when the the address signals 20 and 21 are supplied to the memory 10.

However, it is impossible to specify the test area of the memory by an arbitrary address value since the test area of the memory is specified by limiting the number of bits to be used in the address register 8G in case of generating the regular addresses in the circuits as shown in Figs. 4 and 6.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to provide an address pattern generator capable of freely setting the test area of the memory.

To achieve the above object, the address pattern generator of the present invention comprises a column address generator 4, which receives an add signal 19 from a control circuit 1, an address value 17

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from a first maximum value register 2 and an address value 33 from a first initial-value register 6, and a row address generator 5, which receives the add signal 19 from the control circuit 1, an address value 18 from a second maximum value register 3 and an address value 34 from a second initial-value register 7, characterized in that the arrangement of the column address generator 4 is the same as that of the row address generator 5 and the column address generator 4 comprises a comparator 4E for comparing an address signal to be supplied to the memory 10 with the address value 2 output from the first maximum value register 2 and a selection circuit 4F for selecting the address signal 20 or 21 to be supplied to the memory 10 using a signal output from the comparator 4E.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a view showing an arrangement of an address pattern generator according to the present invention;

Fig. 2 is a view showing an arrangement of a column address generator in Fig. 1;

Fig. 3 is a view showing the relation between the memory cells and addresses of a memory 10 in Fig. 1;

Fig. 4 is a view showing an arrangement of a conventional address pattern generator;

Fig. 5 is a view showing the relation between the memory cells and addresses of a memory 10 in Fig. 4; and

Fig. 6 is a view showing an arrangement of a column address pattern generator 8 in Fig. 4.

DESCRIPTION OF THE PREFERRED EMBODIMENT

The relation between the memory cells and the addresses of the memory 10 in Fig. 1 will be described with reference to Fig. 3. In Fig. 3, the memory 10 comprises memory cells A0 to A24 which are arranged in a 5 x 5 matrice~~s~~. An area 44 to be tested is set aside and a memory cell in that area is selectively exemplified. The area 44 has a regular address pattern in which each memory cell ~~can be accessed by being skipped every other cell such as C1, C2, C3 -----, C9~~.

In order to set aside the area of the memory cell to be tested, a "011" is stored in the first and second maximum value registers 2 and 3 and the "011" is stored in the first and second initial value registers 6 and 7. In order to generate the regular addresses as illustrated in Fig. 3, a "010" is stored in the operation register 4A in the column address generator 4 while a "000" is stored in the operation register 5A in the row address generator 5.

The addresses by which memory cell C1 is accessed at the initialization thereof, i.e., a "001" is supplied to the add register 4G of the column address generator 4 and the address register 5G of the row address generator 5. If the add signal 19 is supplied from the control circuit 1 to the column address generator 4, the "001", i.e., the content of the address register 4G and the "010", i.e., the content of the operation register 4A are added in the adder 4B and the "011", i.e., the result of addition is issued from the adder 4B as the output value 40. The comparator 4E compares the "011", i.e., the content of the first maximum value register 2 with the "011", i.e., the output value 40. In this case, the output value 40 is not greater than the content of the first maximum value register 2, the comparison signal 41 is not issued by the comparator 4E.

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The selection circuit 4F selects the output value 40 when it does not receive the comparison signal 41 and issues the "011" as the selection value 45 which is supplied to the add register 4G. The address register 46 stores the selection value 45 upon reception thereof and then issues the "011" as the address signal 20. Since the row address generator 5 does not receive the comparison signal 41 as a carry signal 35 from the column address generator 4, the row address generator 5 carries out the operation in the same way as the column address generator 4 whereby the address register 5G issues the "001", i.e., the content of the address register 4G as the row address signal 21 as it is. A memory cell C2 is accessed when the "011" is supplied to the memory 10 as the column address signal 20 and the "001" is supplied to the memory 10 as the row address signal 21.

If the next add signal 19 is supplied to the column address generator 4, the "011", i.e., the content of the address register 4G and "010", i.e., the content of the operation register 4A are added in the adder 4B whereby the adder 4B issues a "101", i.e., the result of addition as the output value 40. The comparator 4E compares the "101" of the output value 40 with the "011", i.e., the content of the first maximum value register 2 and issues the comparison signal 41 since the output value 40 is greater than the value representing the first maximum value register 2.

The selection circuit 4F selects the add value 43 upon reception of the comparison signal 41 and issues the add value 43 as a selection value 45, which is supplied to the address register 4G. The add value 43 is the value, ~~which is~~ obtained by adding, carried out in the adder 4D, the "001", i.e., the output value 42 "001" which is the result of subtraction, carried out in the subtracter 4C, between the "101", i.e., the output value

40 and the "011", i.e., the content of the first maximum value register 2 and the "001", i.e., the first initial-value register 6. The result of the addition becomes the "010". The address register 4G stores the selection value 45 and thereafter issues the "010" as the column address signal 20.

Since the comparison signal 41 is supplied from the column address generator 4 to the row address generator 5 as the carry signal 35, the adder 5B carries out the addition including the +1 carry signal. Successively, the row address generator 5 carries out the operation in the same way as the column address generator 4 and issues the "010" as the column address signal 21. A memory cell C3 is accessed when the "010" is supplied to the memory 10 as the column address signal 20 and the "010" is supplied to the memory 10 as the row address signal 21.

Every time the add signal 19 is supplied to the column address generator 4 and the row address generator 5, the outputs of the address signals 20 and 21 vary so that memory cells C4 and C5 are accessed. Likewise, if memory cells C6 to C9 are accessed by skipping every other cell, the addresses by which the memory cell C6 is accessed at the initial state are supplied to the address register 4G of the column address generator 4 and the address register 5G of the row address generator 5 and thereafter the add signal 19 is supplied to the address register 4G of the column address generator 4 and the address register 5G of the row address generator 5.

The arrangement of the address pattern generator according to the present invention will be described with reference to Fig. 1.

It is possible to regularly generate addresses in circuits within a freely set area of memory cells to be tested according to the present invention, so that a program for controlling the generation of address patterns can be made easily.

The address pattern generator comprises a control circuit 1, first and second maximum value registers 2 and 3, a column address generator 4, a row address generator 5, first and second initial-value registers 6 and 7 and a memory 10 which is to be tested. The arrangement of the present invention as illustrated in Fig. 1 is different from the conventional arrangement as illustrated in Fig. Fig. 4 in respect that the former has the first and second initial-value registers 6 and 7 in addition to the arrangement of the latter. The first and second initial-value registers 6 and 7 store therein the minimum values of the addresses by which the memory cell of the test area is accessed. The test area of the memory cell is set when the contents of the maximum value registers 2 and 3 and the contents of the initial-value registers 6 and 7 are supplied to the column address generator 4 and the row address generator 5.

The arrangement of the column address generator 4 will be described with reference to Fig. 2. The arrangement of the column address generator is the same as that of the row address generator. The operation register 4A, the adder 4B and the address register 4G in Fig. 2 are the same as the operation register 8A, the adder 8B and the address register 8G in Fig. 6. The arrangement of the present invention has a subtracter 4C, an adder 4D, a comparator 4E and a selection circuit 4F in addition to the arrangement of the prior art in Fig. 6.

If the add signal 19 is supplied from the control circuit 1 to the adder 4B, the content of the address register 4G and the content of the operation register 4A are added in the adder 4B. The result of addition is supplied as an output value 40 from the adder 4B to the subtracter 4C, the comparator 4E and the selection circuit 4F. The subtracter 4C carries out subtraction between the output value 40 and the address

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value 17 so that the difference therebetween can be obtained. Accordingly, the subtracter 4C receives a borrow signal so that +1 is subtracted extra.

The result of subtraction is supplied as an output value 42 to the adder 4D so that the adder 4D adds the output value 42 and an address value 33 which is the content of the first initial-value register 6 whereby the result of addition is supplied as an add value 43 to the selection circuit 4F. The comparator 4E compares the output value 40 with the address value 17. If the output value 40 is greater than the address value 17, the comparator 4E supplies a comparison signal 41 to the selection circuit 4F and the row address generator 5 while if the output value 40 is less than the address value 17, the comparator 4E does not issue the comparison signal 41.

If the comparison signal 40 is supplied from the comparator 4E to the selection circuit 4F, i.e., if the output value 40 is greater than the address value 17, the selection circuit 4F selects the add value 43. If the comparison signal 40 is not issued from the comparator circuit 4E, i.e., if the output value 40 is the same as or less than the address value 17, the selection circuit 4F selects the output value 40 and issues a selection value 45 which is supplied to the address register 4G. The address signal 4G stores the selection value 45, upon reception thereof from the selection circuit 4F, and thereafter outputs the same as an address signal 20.

In the row address generator 5, if the comparison signal 41 from the column address generator 4 is supplied to the adder 5B as a carry signal 35, the adder 5B receives the signal as a carry of +1 and carries out the addition. The row address generator 5 carries out the operation

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in the same way as the column ~~row~~ address generator 4 so that the address signal 21 is output from the address register 5G.

Every time the add signal 19 is supplied to the column address generator 4 and the row address generator 5, the column address generator 4 and the row address generator 5 issues regularly the address signals 20 and 21 by which the memory cell in a given area of the memory 10 can be accessed.

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